



IBM Research

Flash and Storage Class Memories

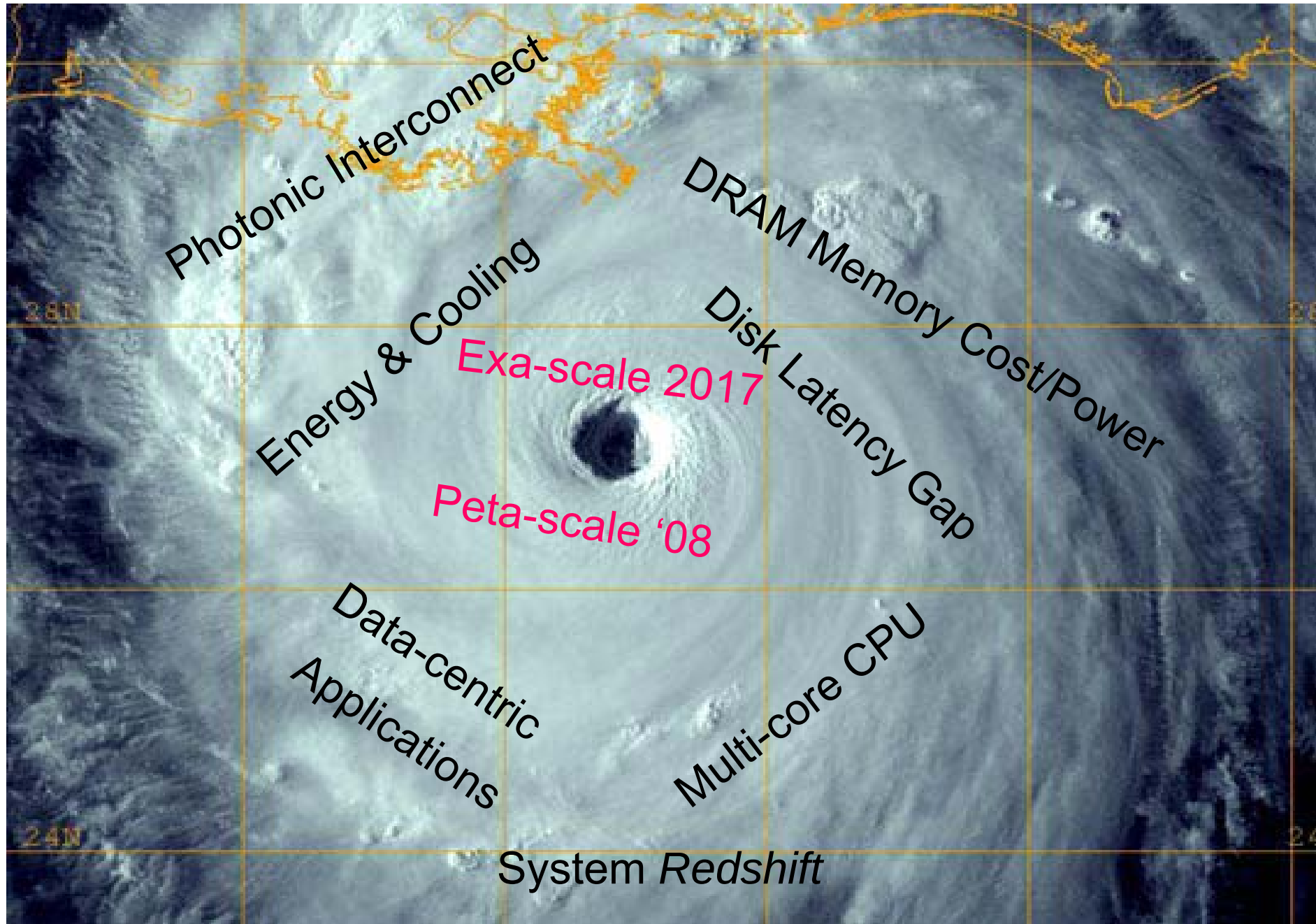
Technology Overview & Systems Impact

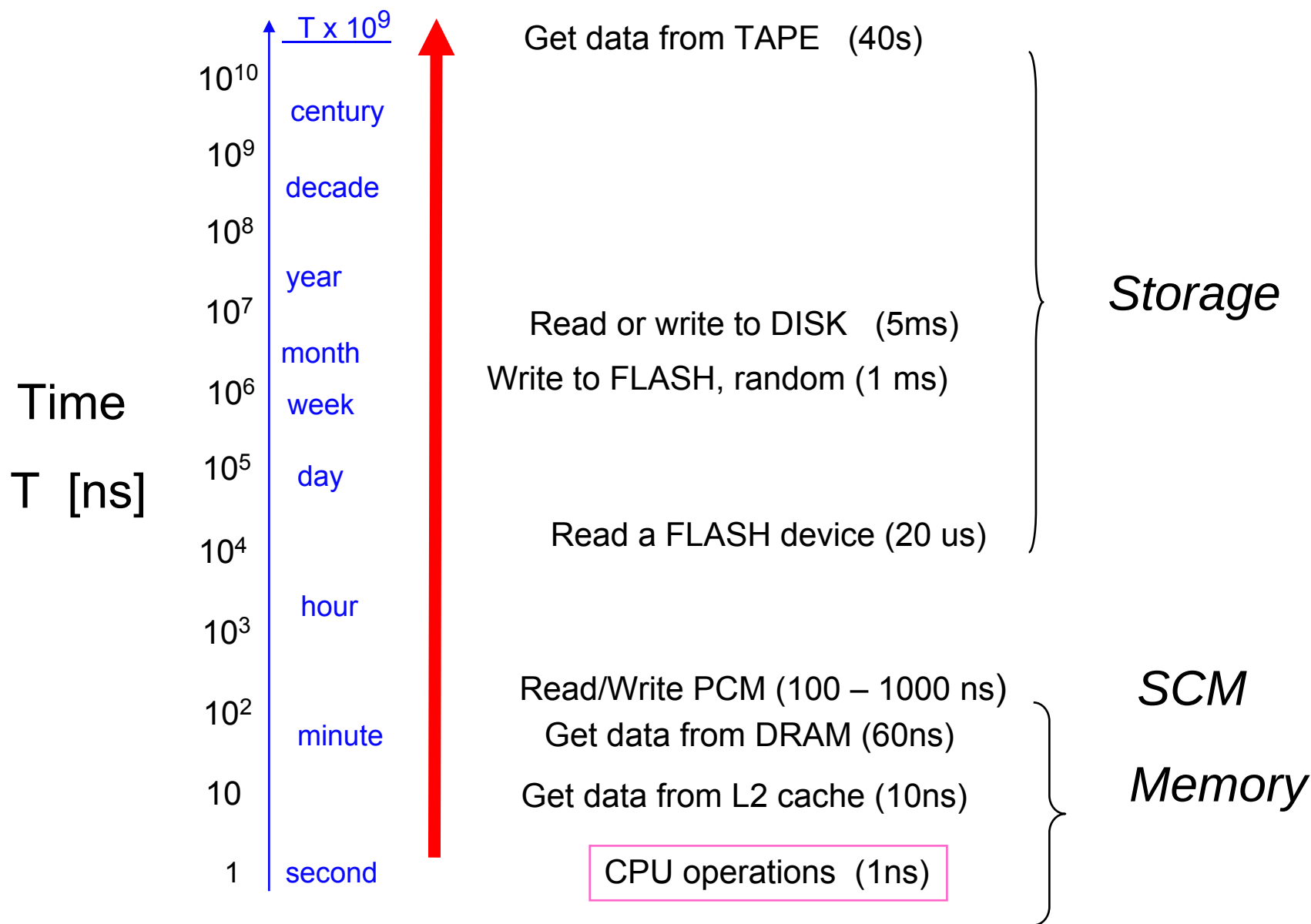
Winfried W. Wilcke

Sr. Manager, Nanoscale Science & Technology;
Program Director, Silicon Valley Projects



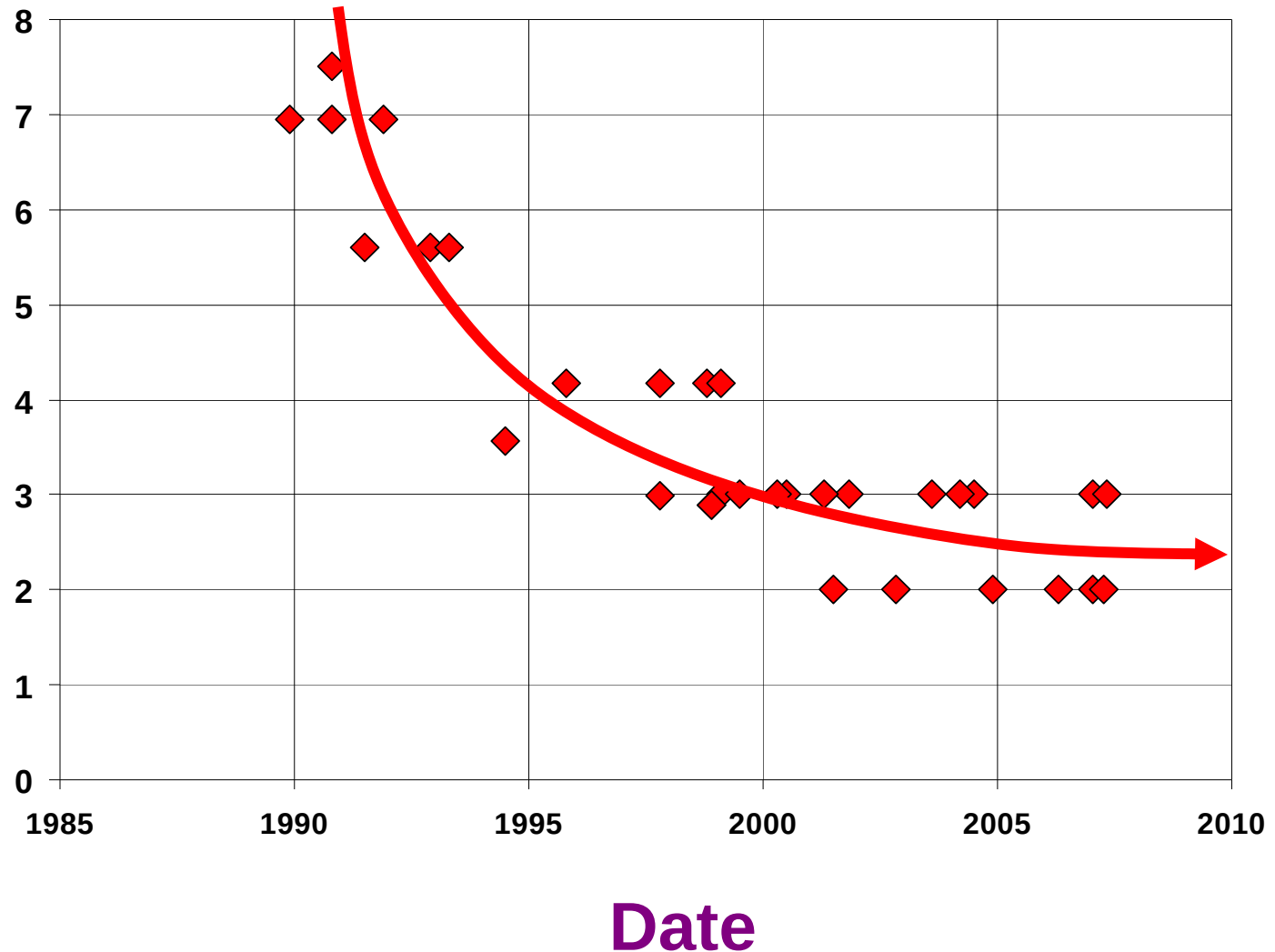
Los Alamos/HECFSIO Conference
August 6, 2008



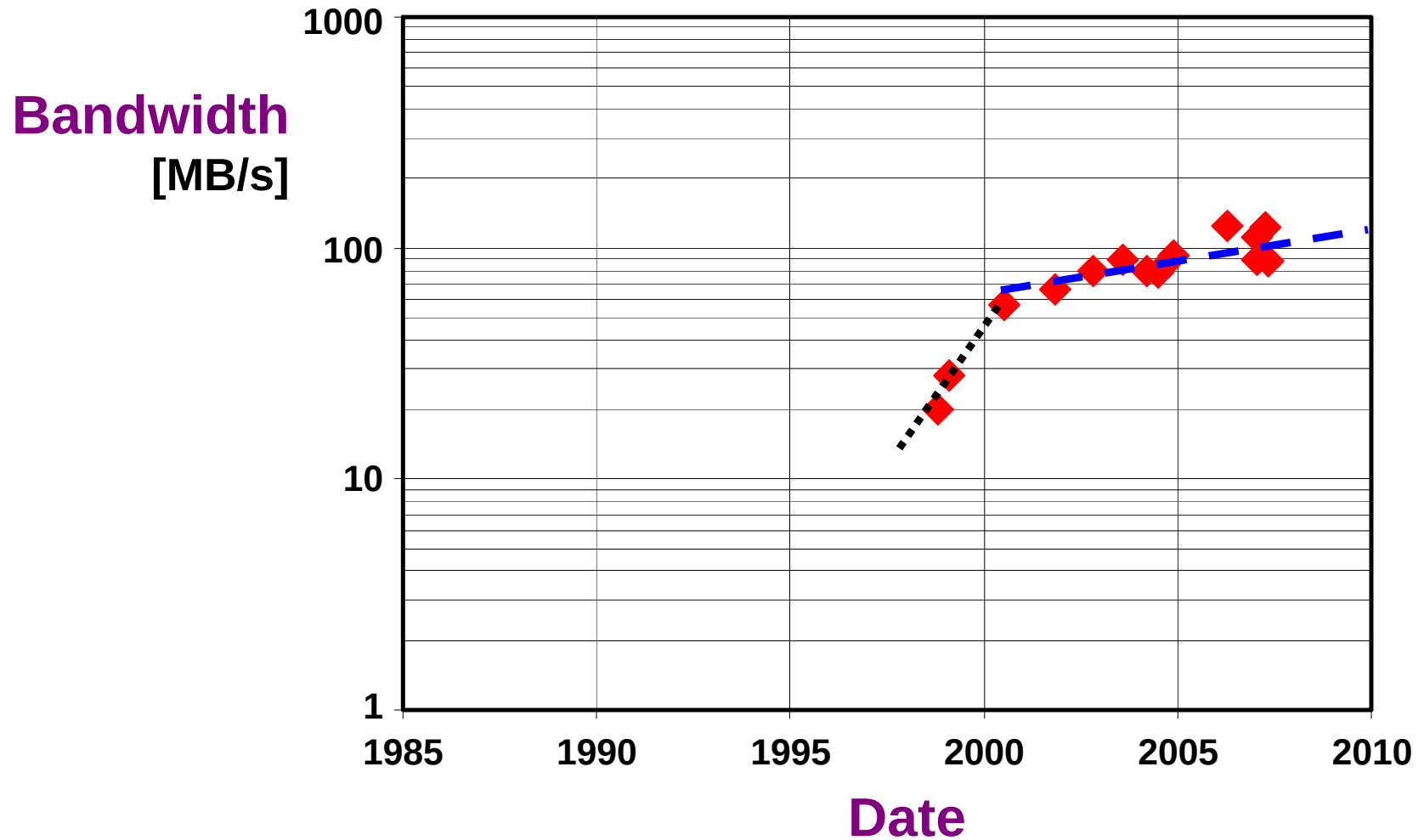


Disk Drive Latency – Little progress...

Latency
[ms]



Disk Drive Maximum Sustained Data Rate



Definition of Storage Class Memory (SCM)

SCM is IBM's term for a new class of data storage and memory devices

SCM blurs the distinction between

- MEMORY (= *fast, expensive, volatile*) and
- STORAGE (= *slow, cheap, non-volatile*)

SCM:

- Solid state, no moving parts
- Short Access times (~ DRAM like, within an order-of-magnitude)
- Low cost per bit (DISK like, within an order-of-magnitude)
- Non-volatile (~ 10 years)

Multiple competing SCM technologies

- Phase Change Memories (PCM), here soon
- Magnetic RAM and magnetic racetrack
- numerous others in various stages of research ...

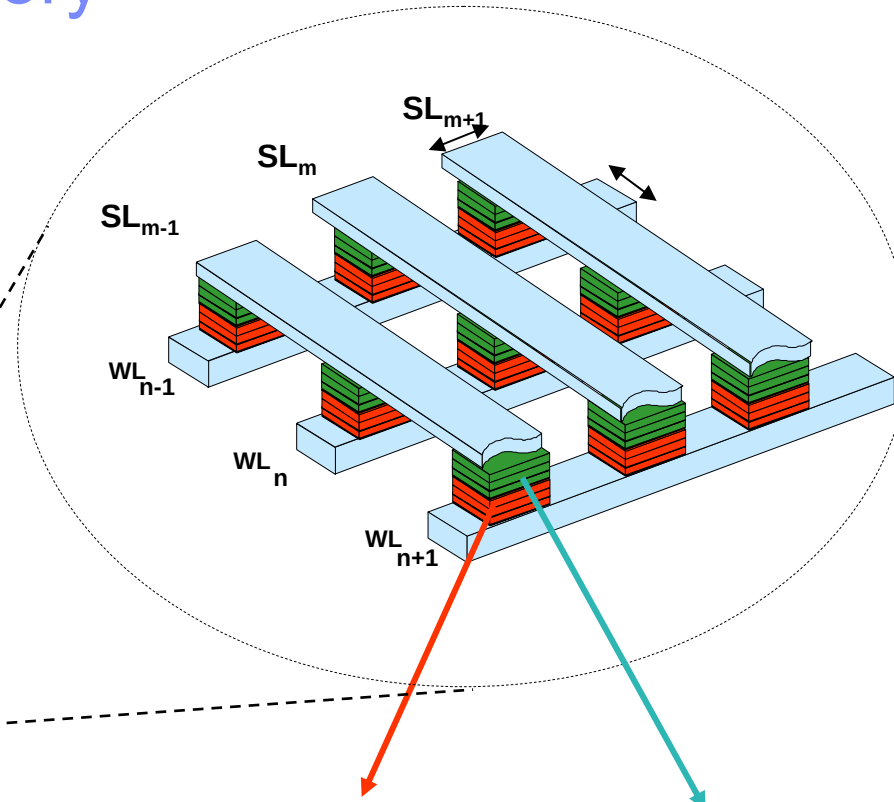
Note: FLASH doesn't quite qualify as SCM (can't be use as memory)

Generic Storage Class Memory

- SCM
- 2D-array of memory elements
- Bistable material at array cross-points
- Phase Change Memory is a (promising) *example* of SCM



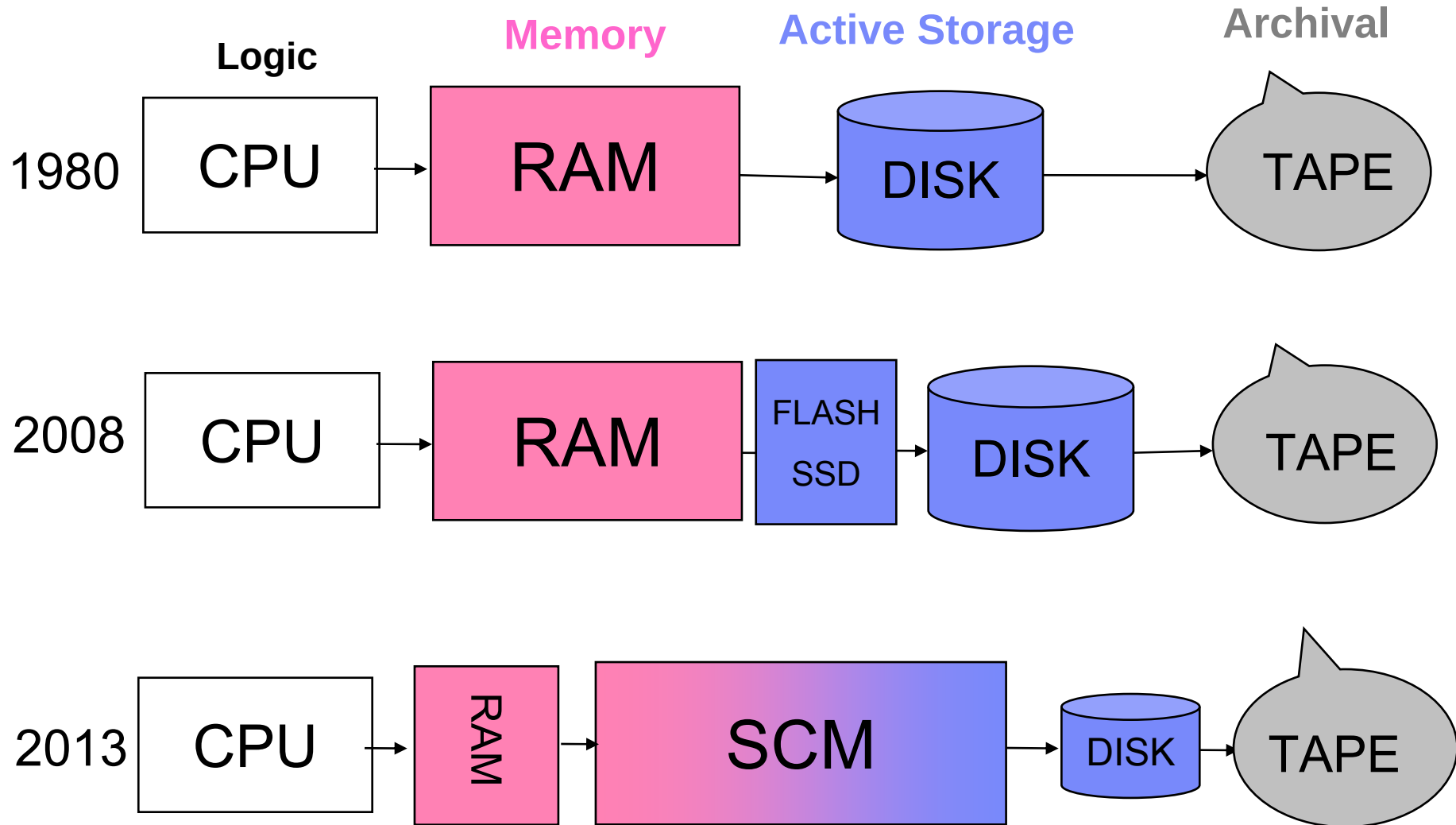
Solid State Memory DIMM



Bistable material

Access control
Device = switch

Evolution of the Memory/Storage (M/S) Stack





SCM Software Impact

Persistent data can be randomly and synchronously(?) addressed

- Huge non-volatile address spaces, memory-mapped DB, persistent objects...
 - Should SCM be used like I/O or like memory or in a totally new way ?
- Software Architecture Questions:
 - Should one make SCM *visible* to applications software?
 - If visible, in which form?
 - New APIs, libraries, memory models, new I/O devices,...
- Databases, Business Intelligence and Streams are first impacted
 - Data-intensive HPC - predictable execution time of complex business analytics - streaming search
 - 21,780 IO/sec for one FusionIO SSD (r/w = 1) vs. ~150 IO/sec for a disk

Future History of Storage Class Memory

Slow Start – but will be a big success eventually

- due to extreme scalability

A Future History of SCM – my version

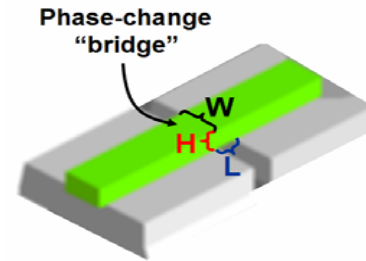
Fundamental advantage of SCM (PCM) is *excellent scalability*

By 2015, SCM (excluding FLASH) could be a \$10-20 Billion chip industry

- Phase Change Memory dominating
- By 2020, SCM revenue may be comparable to DRAM or disks (2x \$40Billion today)

SCM revenues will ramp slowly for the next 3 years, FLASH continues growth

- But, eventually, excellent scaling properties of SCM will outpace FLASH and DRAM
 - Almaden demonstrated PCM bridge with 3nm critical dimension (!)
- Expected sequence of market penetration
 1. FLASH appears in transaction-oriented large systems (2008)
 2. SCM augments FLASH in consumer devices. Initially no software impact (2009)
 3. SCM used in large systems as layer of hierarchy between RAM and disks (2010..)
 4. Much higher write-endurance than FLASH enables memory-like uses (2012...)
 - Boundary of memory and storage blurring, new software paradigms emerging
 5. Widespread acceptance of mixed RAM/SCM/disk stack (2015...)
 6. SCM replaces disks in most applications except for very inactive data (2020...)



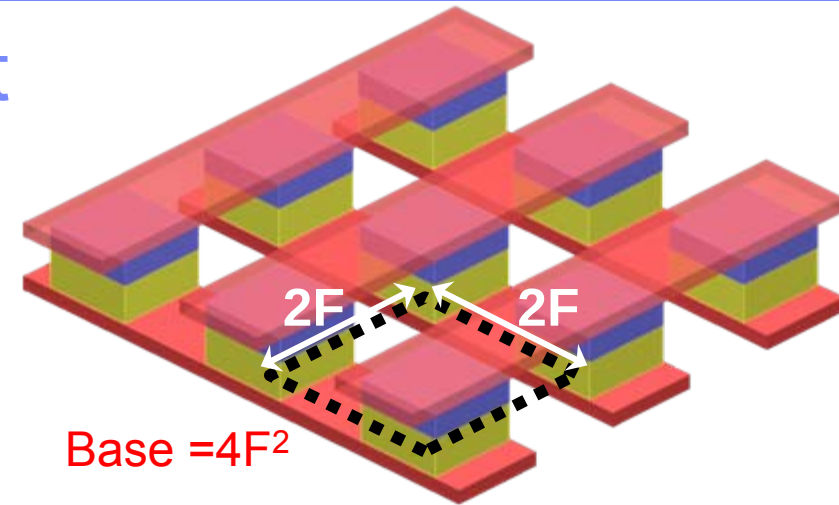
Almaden:

H = 3 nm (!)

W = 20 nm

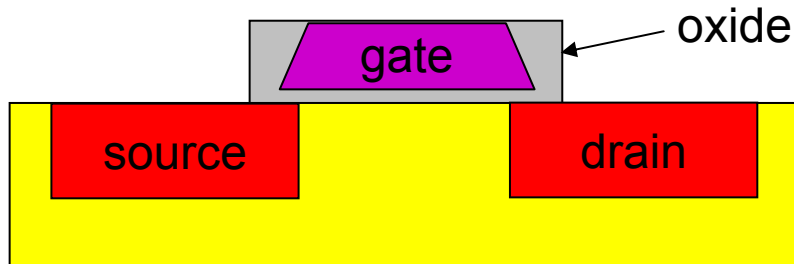
Density is key to low cost/bit

Cost competition between IC,
magnetic and optical
devices comes down to
effective areal density.

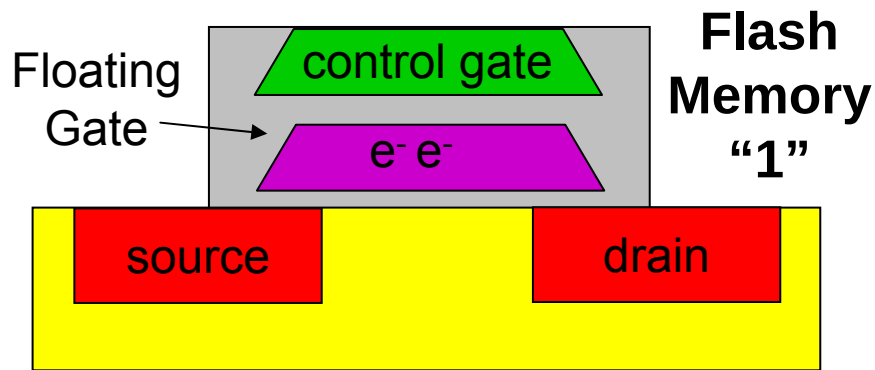


Device	Critical feature-size F	Area (F^2)	Density (Gbit /sq. in)
Hard Disk	80 nm (MR width)	-	200
DRAM	90 nm (half pitch)	8.0	10
NAND (2 bit)	90 nm (half pitch)	3.0	26
NAND (1 bit)	73 nm (half pitch)	4.7	26
Blue Ray	210 nm ($\lambda/2$)	1.5	12

Flash Technology Basics

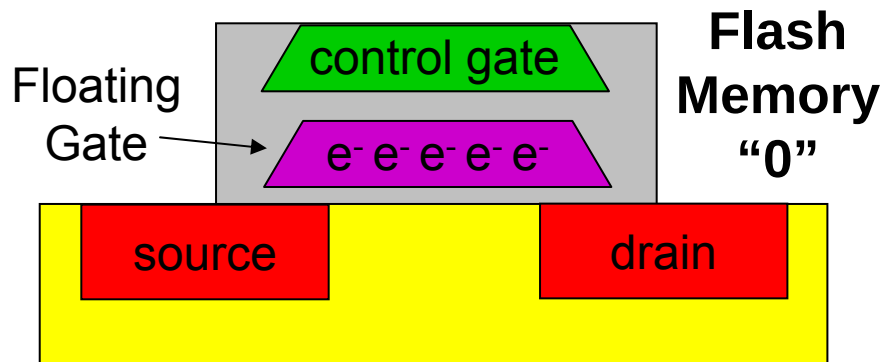


- Based on MOS transistor



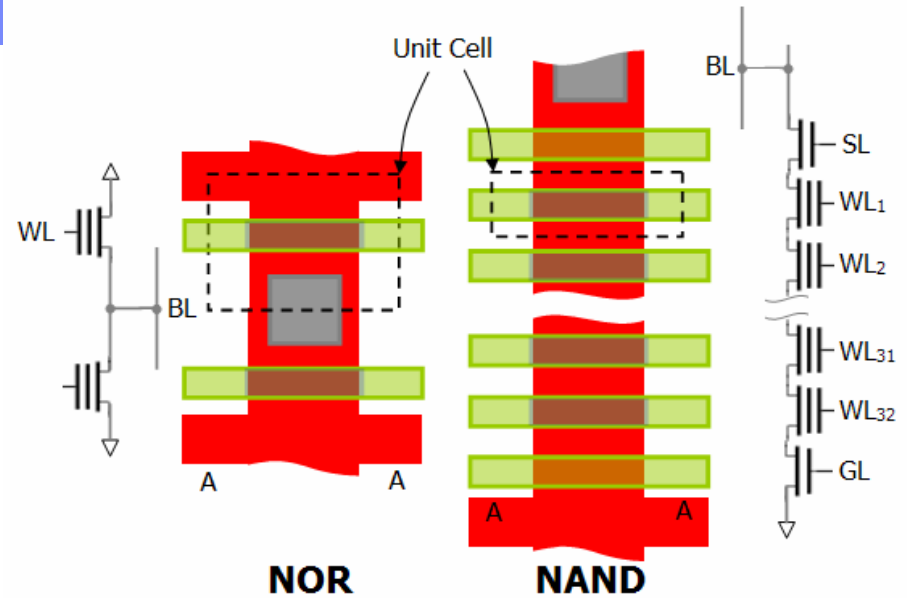
- Transistor gate is redesigned

- Charge is placed on or removed from a 'floating gate'



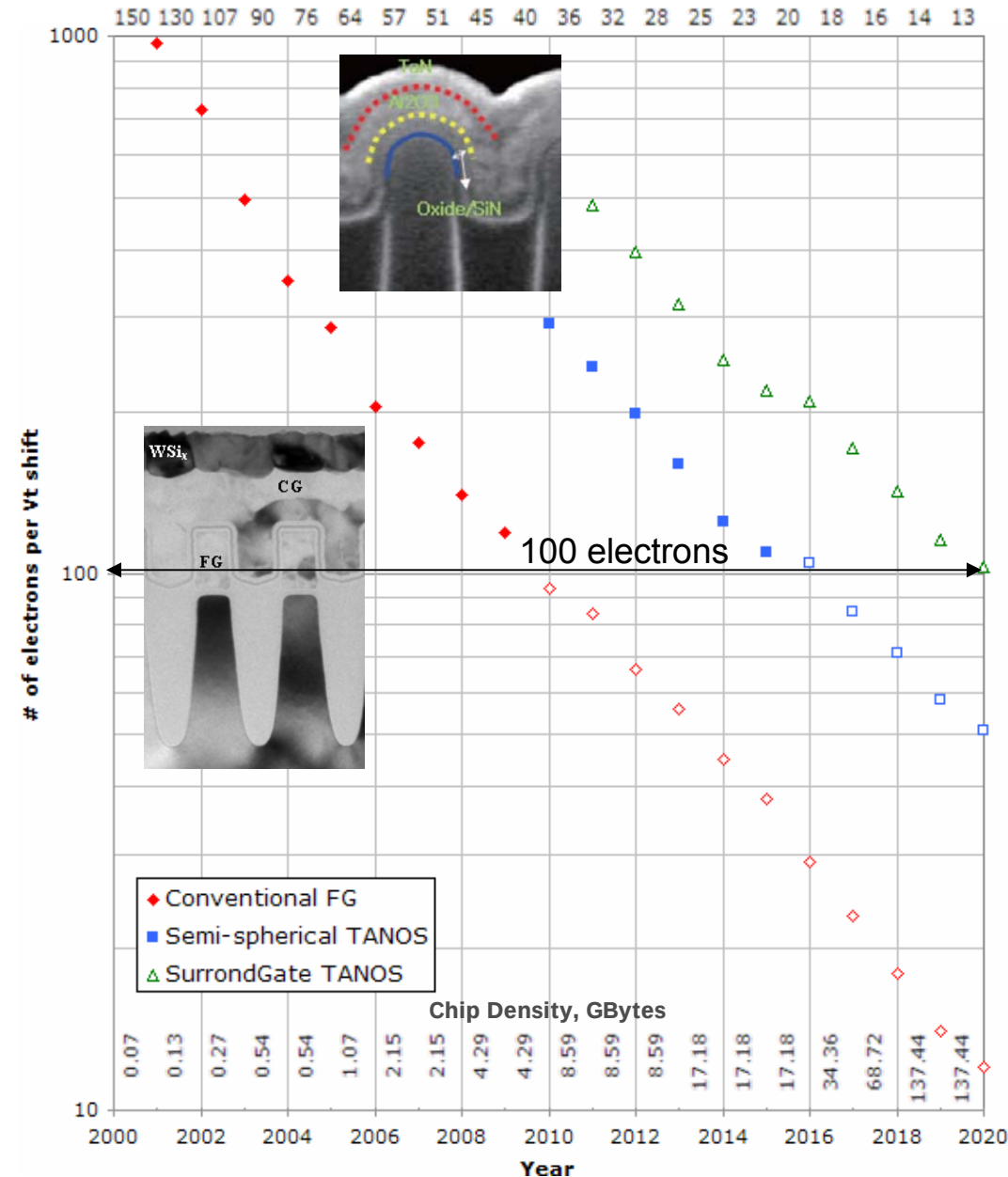
- The threshold voltage V_{th} of the transistor is shifted by the (permanent) presence of this charge
- This can be detected

FLASH memory types and application



	NOR	NAND
Cell Size	9-11 F^2	2 F^2
Read	100 MB/s	18-25 MB/s
Write	<0.5MB/sec	8MB/sec
Erase	750msec	2ms
Market Size (2007)	\$8B	\$14.2B
Main Application	Executable code	Multimedia

FLASH Scaling Challenges: electrical, not physical



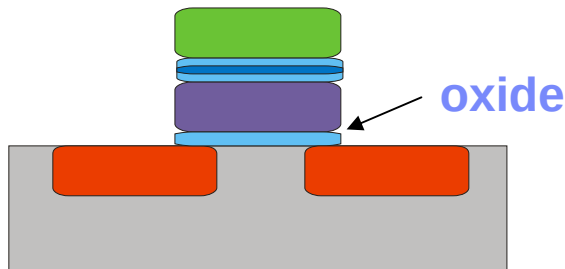
FLASH Challenges

- it's not lithography itself, but...
- not enough electrons
 - **only ~100 e⁻ per level today**
 - Can't even loose one electron per month!
- Electric field stress on gates during programing too high
 - Write endurance drops
 - FLASH never a true SCM
 - (can't be used as a memory)

Source: Chung Lam, IBM

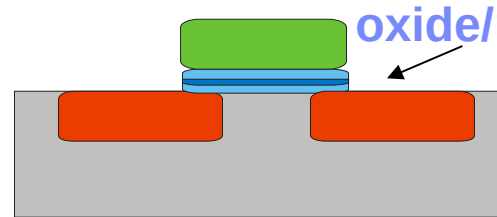
Can **Flash** continue scaling? Maybe.

Feature Size: 40nm → 30nm → 20nm



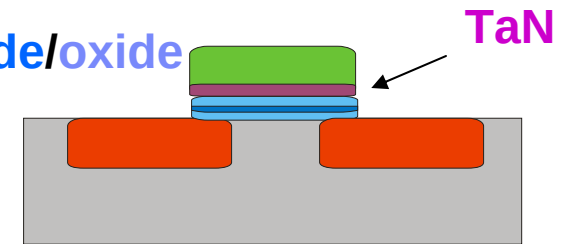
Floating Gate

<40nm ???



SONOS

Charge trapping
in SiN trap layer



TaNOS

Charge trapping
in novel trap layer
coupled with
a metal-gate (TaN)

Hope: maintain the **same** performance and write endurance specs

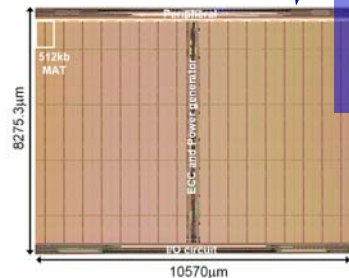
Candidate device technologies

- **Improved Flash**
 - little change expected in write endurance or speed
- **FeRAM** (Ferroelectric RAM)
 - FeFET
- **MRAM** (Magnetic RAM)
 - Racetrack memory
- **RRAM** (Resistive RAM)
 - Organic & polymer memory
- **Solid Electrolyte**
- **PC-RAM** (Phase-change RAM)

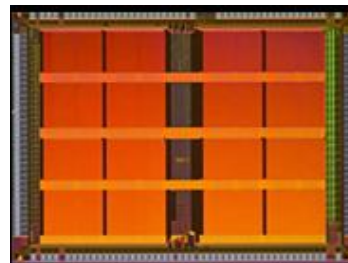
Emerging Memory Technologies

Memory technology remains an active focus area for the industry

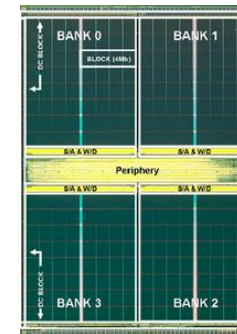
FLASH Extension	FRAM	MRAM	PCRAM	RRAM	Solid Electrolyte	Polymer/Organic
Trap Storage Saifun <i>NROM</i> Tower Spansion Infineon Macronix Samsung Toshiba Spansion Macronix NEC Nano-x'tal Freescale Matsushita	Ramtron Fujitsu STMicro TI Toshiba Infineon Samsung NEC Hitachi Rohm HP Cypress Matsushita Oki Hynix Celis Fujitsu Seiko Epson	IBM Infineon Freescale Philips STMicro HP NVE Honeywel Toshiba NEC Sony Fujitsu Renesas Samsung Hynix TSMC	Ovonyx BAE Intel STMicro Samsung Elpida IBM Macronix Infineon Hitachi Philips	IBM Sharp Unity Spansion Samsung	Axon Infineon	Spansion Samsung TFE MEC Zettacore Roltronics Nanolayer



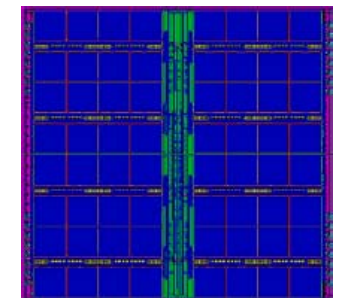
64Mb FRAM (Prototype)
0.13µm 3.3V



4Mb MRAM (Product)
0.18µm 3.3V

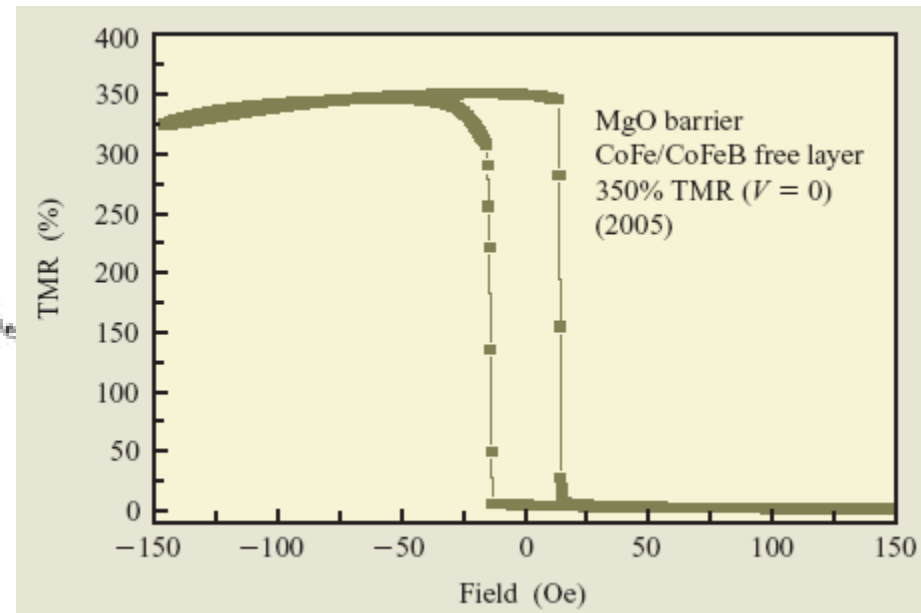
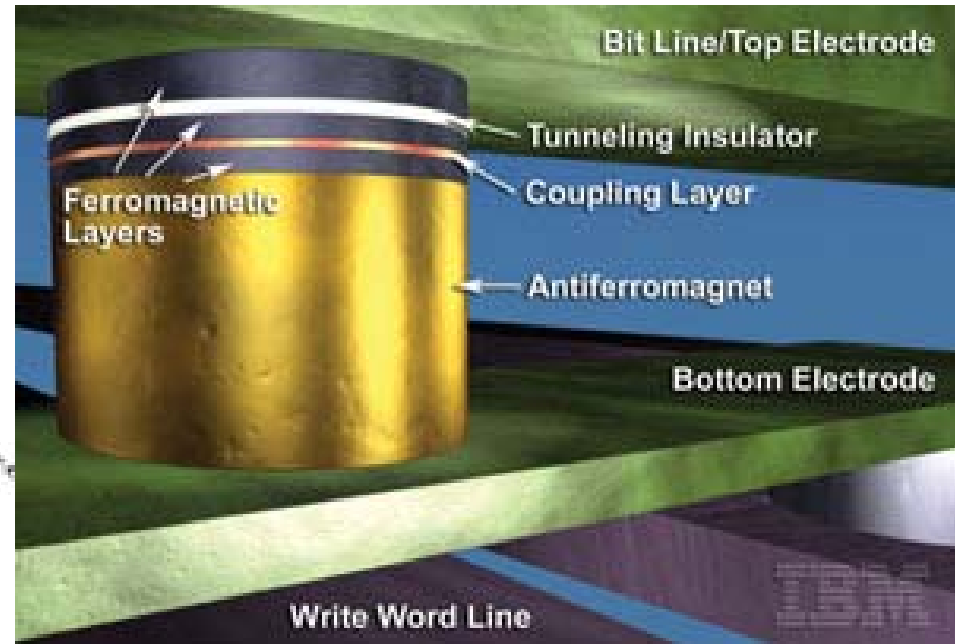
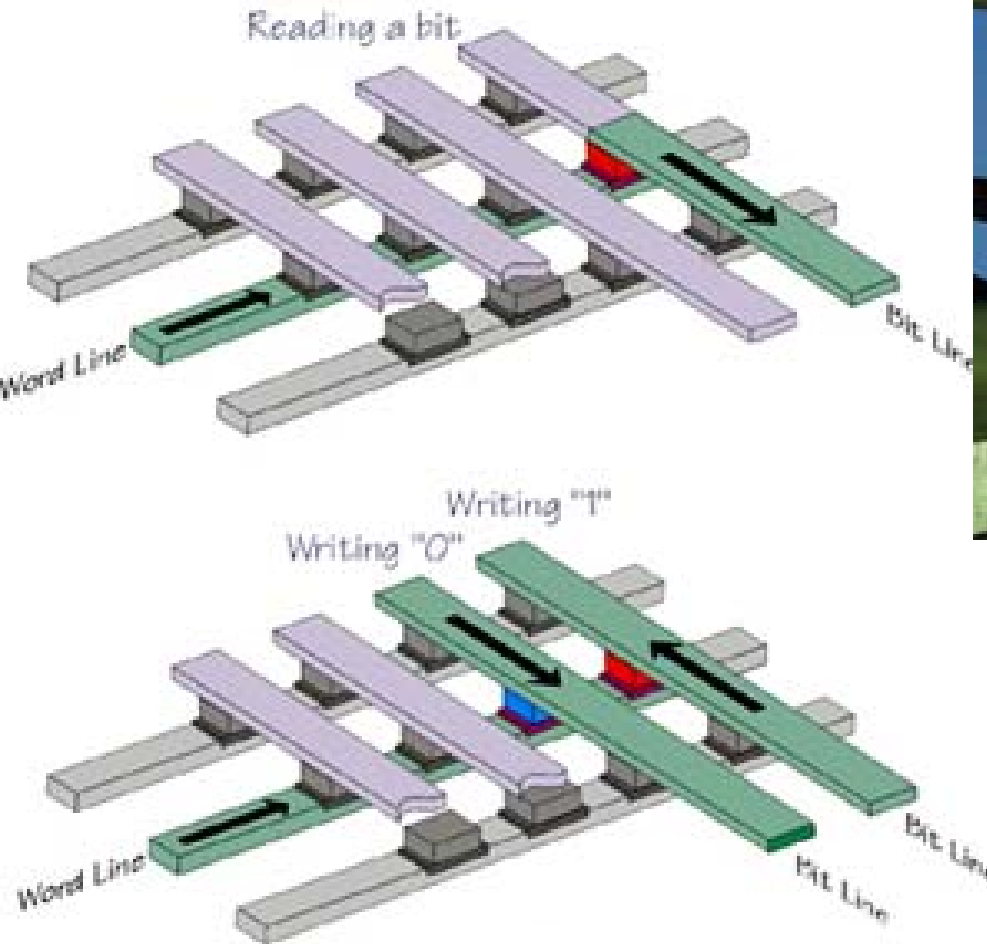


512Mb PRAM (Prototype)
0.1µm 1.8V



4Mb C-RAM (Product)
0.25µm 3.3V

MRAM (Magnetic RAM)



- + No write endurance issues
- Too big and scaling problems

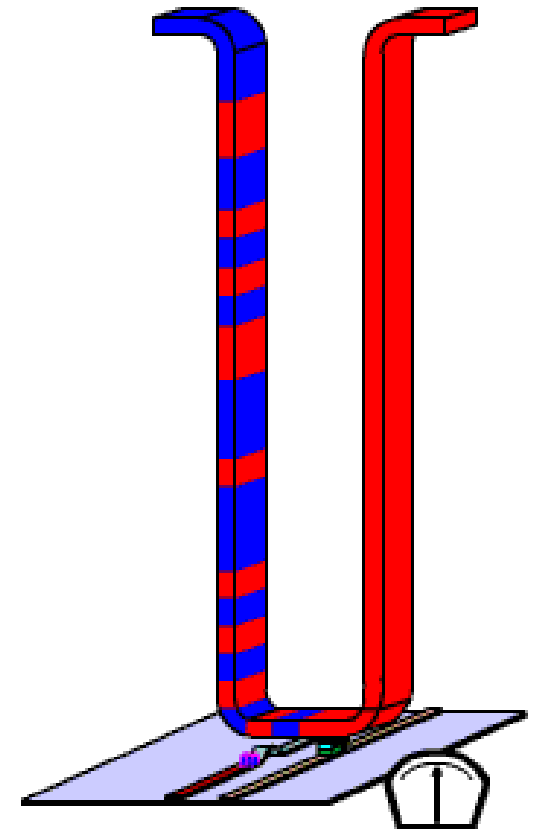
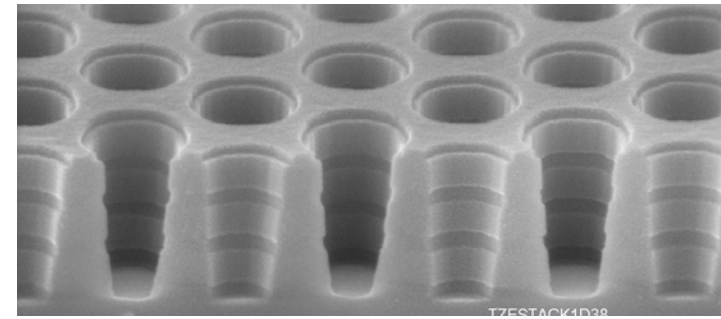
[Gallagher:2006]

Magnetic Racetrack Memory

- Need deep trench with notches to “pin” domains
- Need sensitive sensors to “read” presence of domains
- Must insure a moderate current pulse moves every domain one and only one notch

Promise (10-100 bits/F²) is enormous...

but we're still working on the basic understanding of the physical phenomena...



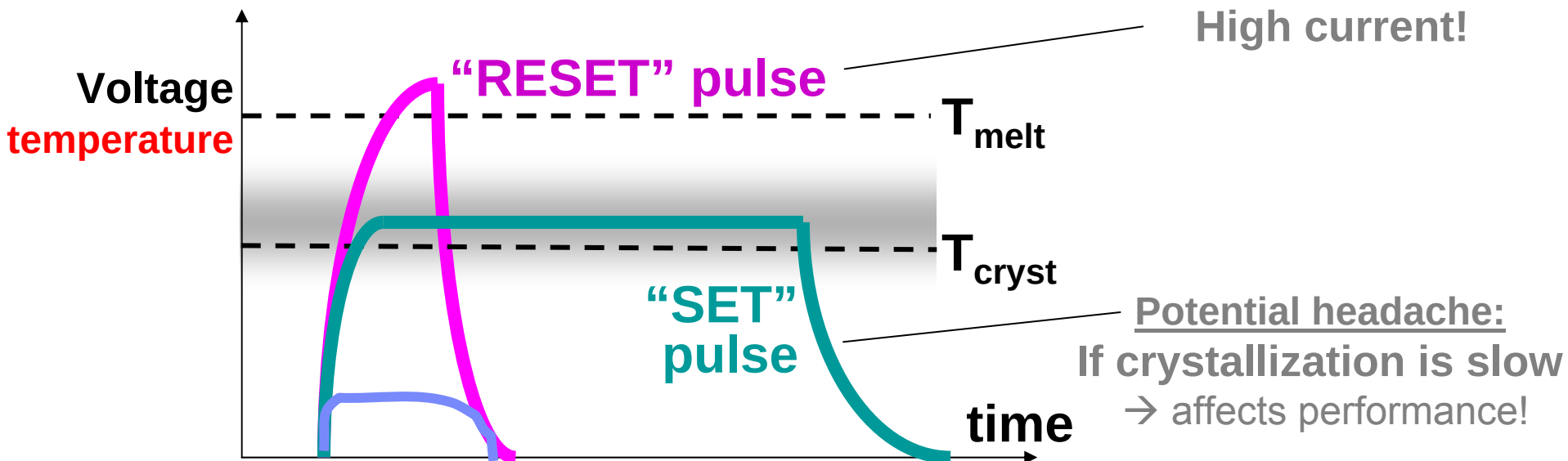
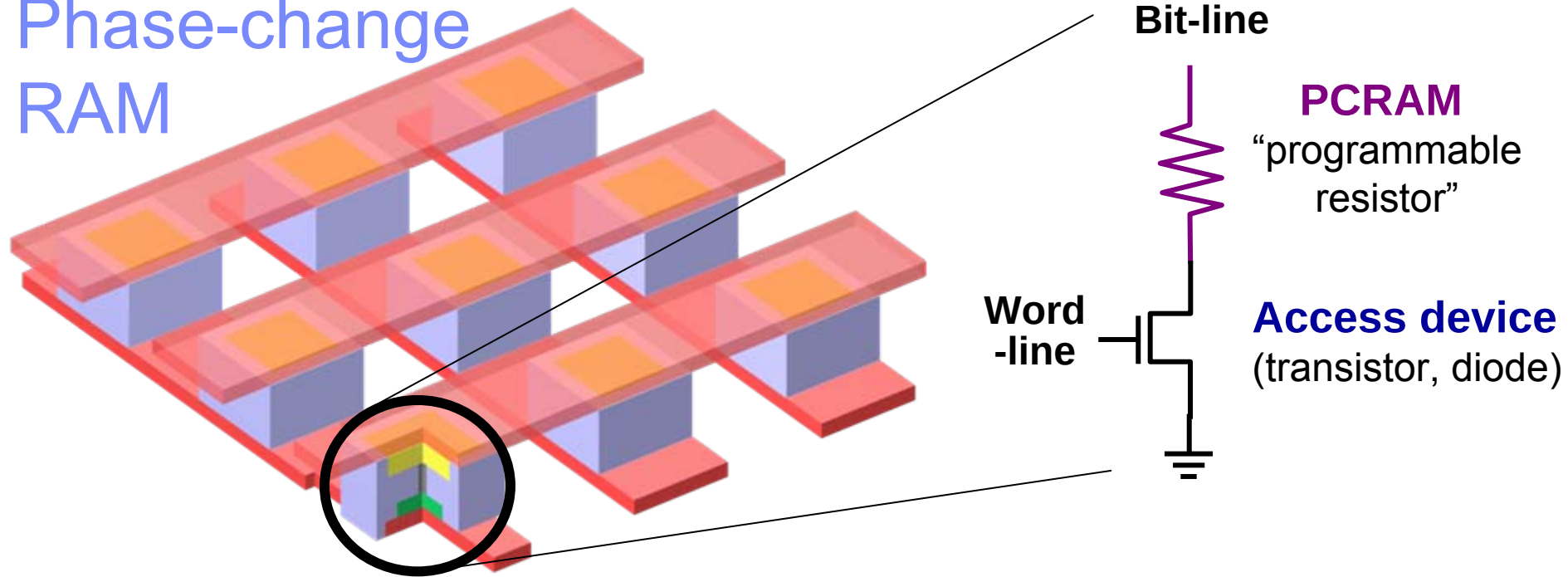
Phase Change Memory

- Currently, leading contender for first true Storage Class Memory
 - Samsung
 - IBM
 - Intel / STMicroelectronics spun out Numonyx
 - BAE (space uses)
- 0.5 Gigabit PCM chips being sampled now

PCM Basic Concepts

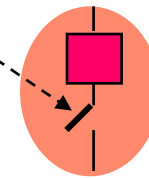
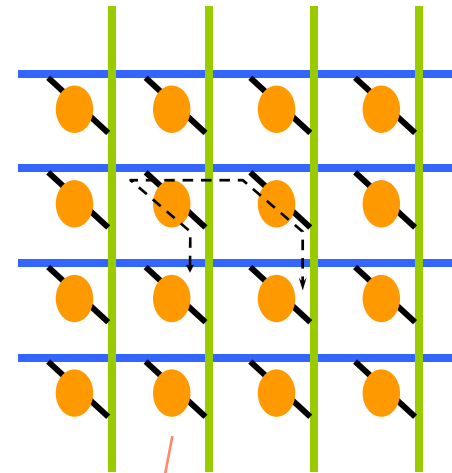
- ***Use two distinct solid phases of a metal alloy to store a bit***
- **Ge-Sb-Te exists in a (quasi)stable amorphous and a stable crystalline phase**
 - Phases have very different electrical resistances – ratio of 1:100 to 1:1000 (!)
 - They also have different optical reflectivity – used today in writable CD/DVD
- **Transition between phases by controlled heating and cooling**
 - **Write '0' (RESET)** : short (10ns) intense current pulse melts alloy crystal
=> amorphous = high resistance
 - **Write '1' (SET)** : longer (50ns) weaker current pulse re-crystalizes alloy
=> crystalline = low resistance
 - **Read** : short weak pulse senses resistance, but doesn't change phase

Phase-change RAM



Crosspoint Memory Array and Access Control

- An on-off switch is needed in series with memory element at every crosspoint node to prevent sneak leakage paths.
 - Also called *access control device*
- **4 Options for *Access control device***
 1. Transistor – MOS type
 2. Transistor – Bipolar Junction type
 3. Diode – conventional Silicon pn
 4. Diode - novel materials



= blob of memory material
plus a on-off switch

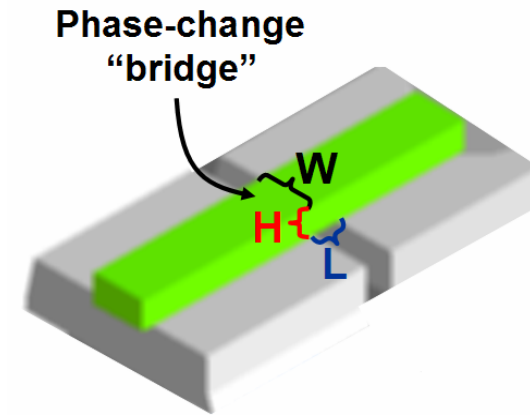
Ultrascaling of Phase-Change Memory

- Prototype memory device with ultra-thin (**3nm**) films – IBM 2006

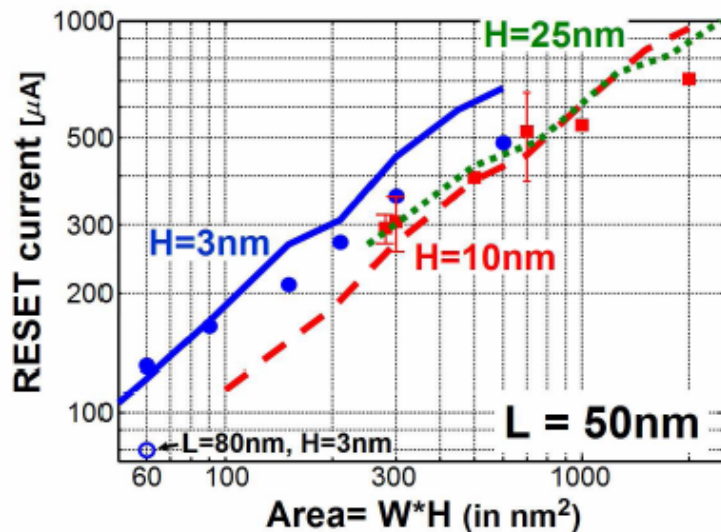


- $3\text{nm} * 20\text{nm} \rightarrow 60\text{nm}^2$
→ phase-change scales

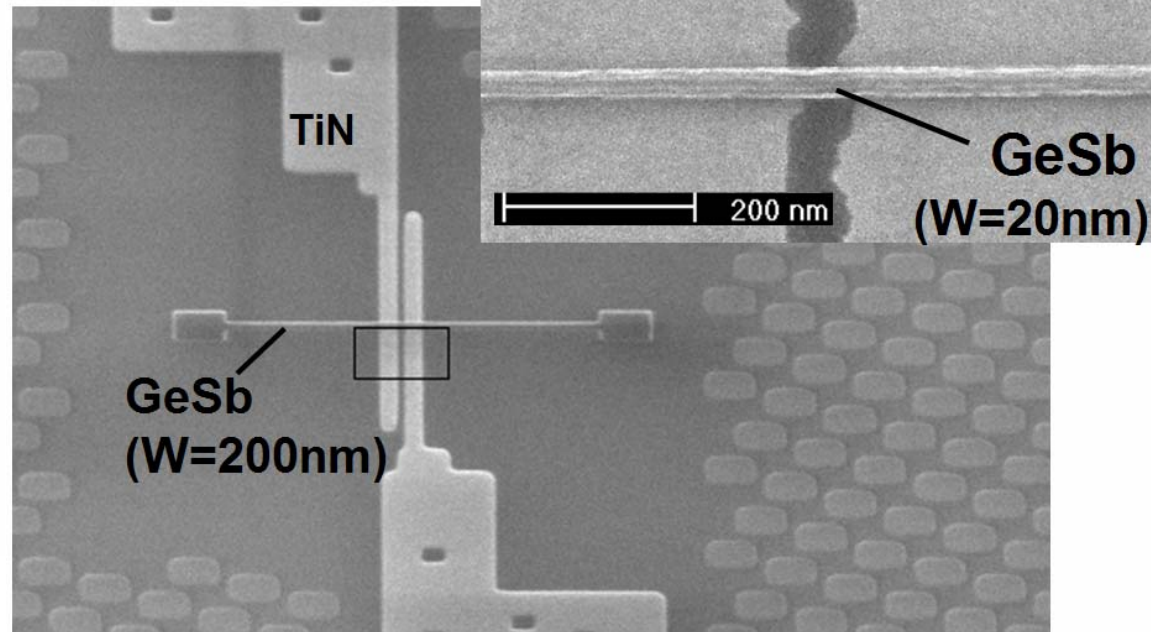
- Fast** (<100ns SET)
- Low current** (< 100 μ A RESET)



W defined by **lithography**
H by **thin-film deposition**



Current scales with area



[Chen:2006]

PCM for ultra-high density: Scaling + Layers + Multi-bits/cell

At the 32nm node in 2013, for an array size of 66 mm²

	<u>density</u>	<u>chip</u>
Base ($4F^2$)	24 Gb/cm ²	→ 16Gb

2x ($2F^2$)	48 Gb/cm ²	→ 32Gb
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e.g., 2 layers or 2 bits per cell

4x ($1F^2$)	96 Gb/cm ²	→ 64Gb
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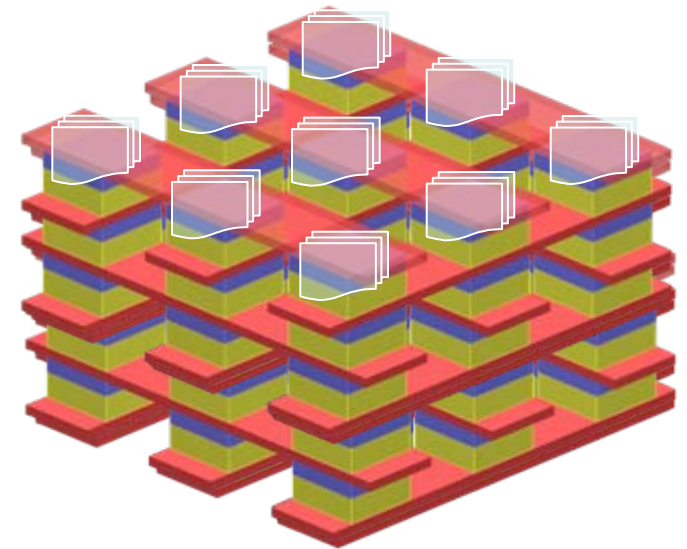
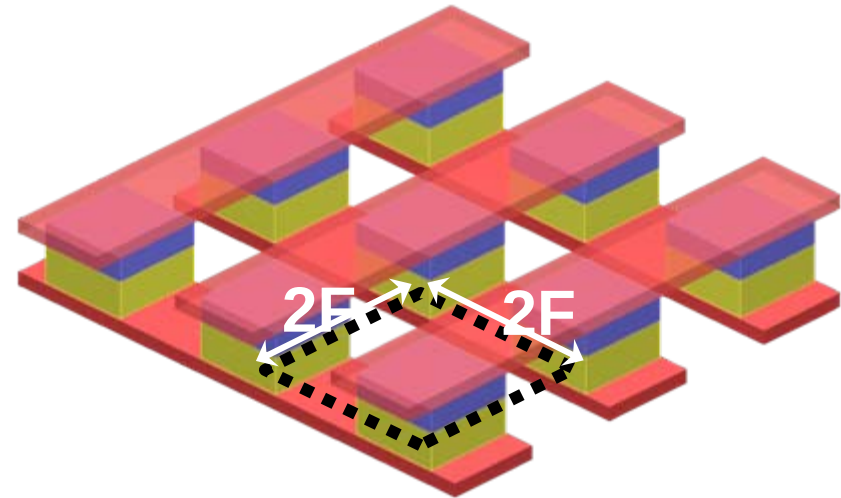
e.g., 4 layers or 2 layer and 2 bits per cell

8x($F^2/2$)	192 Gb/cm ²	→ 128Gb
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e.g., 4 layers and 2 bits/cell

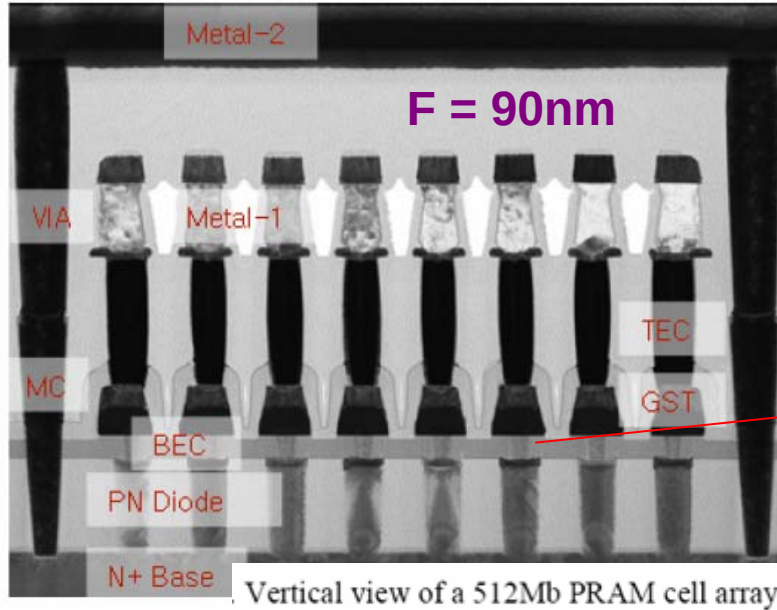
16x ($F^2/4$)	384 Gb/cm ²	→ 256Gb
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e.g., 4 layers, 4 bits/cell



Terabit challenge ☺

PCM state-of-the-art

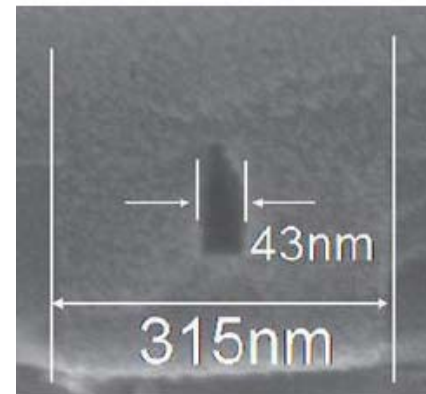
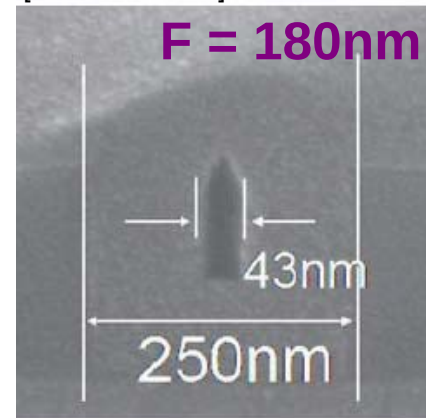


Samsung:

- diode $\rightarrow$ more current
- 90nm process



[Breitwisch:2007]



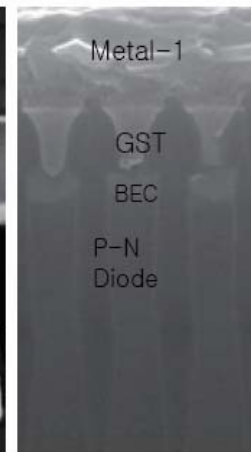
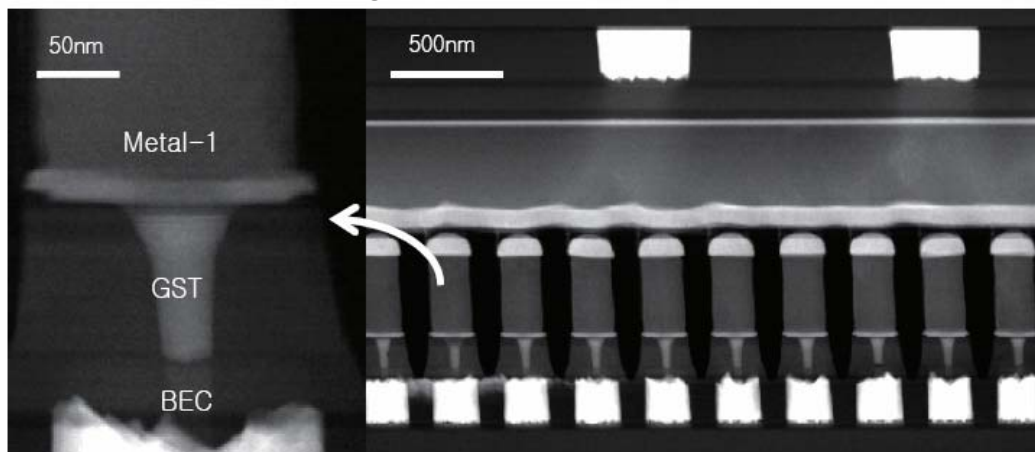
IBM/Macronix/Qimonda:

Sub-lithographic
PCM features

[Lee:2007 VLSI]

[Oh:2006]

Samsung: CVD process fills deep holes



Phase Change Memory Chip – Specs (circa 2012)

- 16 - 128 Gbits
- (chip level) Write endurance of $\sim 10^8$
- 50 – 100 ns Read Latency
- 200...500 ns random Write Latency (performance PCM)
- 2..3 μ s random Write Latency (density optimized PCM)
- Bandwidth 100 – 500 MB/s per chip (power/bandwidth trade-off)
- wild card: Ternary CAM application

Summary

- Disks continue to improve in \$/GB, but barely in performance
- Faster devices are needed, especially for latency critical uses
 - Data-intensive applications gain on compute-intensive applications
- FLASH today, Storage Class Memory soon (2011)
 - *Phase Change Memory* good contender for Storage Class Memory
 - Others are Magnetic RAM and Solid Electrolyte
 - PCM superior to FLASH in latency (especially writes) and write endurance
 - FLASH will have electrical scaling problems past 32nm feature size
- What are the software implications of SCM?
 - Long term, it's impact may be comparable to the 1960's transition from tape to disk
 - It blurs the crisp boundary between memory and storage
 - Eventually, we will need to completely rethink the memory/storage stack



IBM Research

Thank you!

